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10/531,582	10/12/2005	Shinsuke Harada	270968US2X PCT	1837
22850	7590	06/07/2010	EXAMINER	
OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, L.L.P.			KIM, JAY C	
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ALEXANDRIA, VA 22314				
			ART UNIT	PAPER NUMBER
			2815	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentdocket@oblon.com
oblonpat@oblon.com
jgardner@oblon.com

Office Action Summary	Application No. 10/531,582	Applicant(s) HARADA ET AL.	
	Examiner JAY C. KIM	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 April 2010.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 13-22 and 27 is/are pending in the application.
- 4a) Of the above claim(s) 18, 19 and 22 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 13-17, 20, 21 and 27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 May 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This Office Action is in response to Amendment filed April 27, 2010.

Claim Objections

1. Claims 13-16 and 27 are objected to because of the following informalities:

In claims 13-16 and 27, "high concentration" or "low concentration" should be replaced by "high impurity concentration" or "low impurity concentration", respectively, to clearly define that the high or low concentration refers to a high or low impurity concentration.

On line 5 of claim 13, "silicon carbide" should be inserted before "substrate".

In claim 27, "an upper surface" should be replaced by "the upper surface" on line 6, and "high concentration" should be replaced by "low impurity concentration" on line 7, because low impurity concentration gate regions should include the low impurity concentration gate region.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 13, 15, 17, 20, 21 and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Okuno et al. (US 6,165,822) (alternate interpretation).

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Regarding claim 13, Okuno et al. disclose a silicon carbide semiconductor device (Fig. 7C) comprising a lower deposition film (whole n^- region 2 and regions 30a and 30b) which is formed of a single layer of silicon carbide (col. 5, lines 16-18) of a first conductivity type (n-type), and which has lower impurity concentration (n^-) than a high concentration (n^+) silicon carbide substrate (1) (col. 5, lines 10-11) of the first conductivity type (n-type) and which is formed on a surface (top or bottom surface) of the substrate (1), a high concentration gate region (30a or 30b) (col. 8, lines 15-16) of a second conductivity type (p-type) selectively formed across from an upper surface (upper surface/boundary of 2 in contact with 5, 3a and 3b) to an interior of the lower deposition film, the high concentration gate region (30a or 30b) being adjacent to a non-implanted portion (portion of 2 between 3a and 3b) that is an exposed part of the upper surface of the lower deposition film (whole n^- region 2 and regions 30a and 30b), an upper deposition film (3a, 3b, 4a, 4b and 5) formed on the lower deposition film in which the high concentration gate region (30a or 30b) is formed, wherein the upper deposition film comprises a low concentration gate region (3a or 3b) (col. 5, line 23) of the second conductivity type (p-type) directly deposited on a surface of the high concentration gate region (30a or 30b) of the second conductivity type (p-type) and having a lower concentration (p^-) than the high concentration gate region (p^+ , 30a or 30b), a high concentration source region (4a or 4b) (col. 8, line 4) of the first conductivity type (n-type) selectively formed on part of an upper surface of the low concentration gate region (3a or 3b) of the second conductivity type (p-type) and being more heavily doped (n^+) than the low concentration (p^-) gate region (3a or 3b) of the second conductivity type (p-

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type), and a low concentration base region (5) (col. 5, lines 28-29) of the first conductivity type (n-type) formed on the non-implanted portion (portion of 2 between 3a and 3b) and having a greater width than the non-implanted portion and being doped less (n^-) than the high concentration (n^+) source region (4a or 4b) of the first conductivity type (n-type), a gate insulation film (7) (col. 8, line 26) formed on at least a surface of the upper deposition film (3a, 3b, 4a, 4b and 5), a gate electrode (8) (col. 8, line 43) formed via the gate insulation film (7), a drain electrode (11) (col. 8, line 53) having a low-resistance contact connection with a backside of the silicon carbide substrate (1) of the first conductivity type (n-type), and a source electrode (10) (col. 8, line 53) having a low-resistance contact connection with part of the high concentration source region (4a or 4b) of the first conductivity type (n-type) and the low concentration gate region (3a or 3b) of the second conductivity type (p-type).

Regarding claims 15, 17, 20, 21 and 27, Okuno et al. further disclose that the low concentration base region (5) of the first conductivity type (n-type) has a lower impurity concentration (n^-) than the high concentration (p^+) gate region (30a or 30b) of the second conductivity type (p-type) (claim 15), the upper deposition film (3a, 3b, 4a, 4b and 5) is constituted of silicon carbide (col. 5, lines 28-31 and 47-48) (claim 17), in terms of crystal Miller index the surface (top or bottom surface) of the silicon carbide substrate (1) of the first conductivity type (n-type) is a plane that is parallel to a (11-20) plane (col. 5, lines 11-14) (claim 20) or a plane that is parallel to a (000-1) plane (claim 21), and high concentration gate regions (30a and 30b) including the high concentration gate region (30a or 30b) of the second conductivity type (p-type) are formed on both

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sides of the non-implanted portion (portion of 2 between 3a and 3b) so that the non-implanted portion will be formed in an intermediate part of the upper surface of the lower deposition film (whole n⁻ region 2 and regions 30a and 30b), low concentration gate regions (3a and 3b) including the low concentration gate region (3a or 3b) of the second conductivity type (p-type) are respectively directly deposited on surfaces of the high concentration gate regions (30a and 30b) of the second conductivity type (p-type) on both sides of the base region (5) of the first conductivity type (n-type), and source regions (4a and 4b) including the source region (4a or 4b) of the first conductivity type (n-type) are respectively formed on parts of upper surfaces of the low concentration gate regions (3a and 3b) of the second conductivity type (p-type) on both sides of the base region (5) of the first conductivity type (n-type) (claim 27).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 13, 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (US 5,893,736) in view of Okuno et al. (US 6,165,822).

Regarding claim 13, Lee et al. disclose a semiconductor device (Fig. 1) comprising a lower deposition film (20) (col. 1, line 47) which is formed of a single layer of a semiconductor material of a first conductivity type (n-type) (col. 3, lines 18-21), and

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which has lower impurity concentration than a high concentration semiconductor substrate (10) (col. 3, lines 26-28) and which is formed on a surface of the substrate (10) (col. 1, line 47), a high concentration gate region (p^+ region) of a second conductivity type (p-type) selectively formed across from an upper surface to an interior of the lower deposition film (20), the high concentration gate region (p^+ region) being adjacent to a non-implanted portion (arbitrary portion of 20 between two p^+ regions) that is an exposed part of the upper surface of the lower deposition film (20), an upper deposition film (22) (col. 1, lines 47-49) formed on the lower deposition film (20) in which the high concentration gate region (p^+ region) is formed, wherein the upper deposition film (22) comprises a low concentration gate region (50, p^- region) (col. 1, line 49) of the second conductivity type (p-type) directly deposited on a surface of the high concentration gate region (p^+ region) of the second conductivity type (p-type) and having a lower concentration (p^-) than the high concentration gate region (p^+ region), a high concentration source region (n^+ , 52) (col. 1, line 49) of the first conductivity type (n-type) selectively formed on part of an upper surface of the low concentration gate region (50) of the second conductivity type (p-type) and being more heavily doped (n^+) than the low concentration (p^-) gate region (50) of the second conductivity type (p-type), and a low concentration base region (portion of 22 between two p^- regions) formed on the non-implanted portion (arbitrary portion of 20 between two p^+ regions) and having a greater width than the non-implanted portion, because the arbitrary portion of 20 between two p^+ regions may be selected to be narrower than the region of 22 between two p^- regions, a gate insulation film (60) (col. 4, line 59) formed on at least a surface of

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the upper deposition film (22), a gate electrode (70) (col. 4, lines 59-60) formed via the gate insulation film (60), a drain electrode (74) (col. 1, line 50) having a low-resistance contact connection with a backside of the semiconductor substrate (10) of the first conductivity type (n-type), and a source electrode (72) (col. 1, lines 49-50) having a low-resistance contact connection with part of the high concentration source region (52) of the first conductivity type (n-type) and the low concentration gate region (50) of the second conductivity type (p-type).

Lee et al. differ from the claimed invention by not showing that the semiconductor device is a silicon carbide semiconductor device, wherein the single layer of the semiconductor material is a single layer of silicon carbide, the semiconductor substrate is a silicon carbide substrate, and the low concentration base region is of the first conductivity type, and is doped less than the high concentration source region of the first conductivity type.

Okuno et al. disclose a silicon carbide semiconductor device (Fig. 7C) comprising a silicon carbide substrate (1) (col. 5, lines 10-11), a single layer (2) of silicon carbide (col. 5, lines 16-18), an n-type low concentration base region (portion of 2 between 3a and 3b), wherein the low concentration base region is doped less than an n-type high concentration source region (4a or 4b) (col. 8, line 4).

Since both Lee et al. and Okuno et al. teach a semiconductor device, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the semiconductor substrate and layer disclosed by Lee et al. may be formed of silicon carbide as disclosed by Okuno et al., the low concentration base region

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disclosed by Lee et al. may be of the first conductivity type, and the n-type high concentration source region disclosed by Lee et al. may be doped more than the low concentration base region, because silicon carbide is a well-known semiconductor material used in manufacturing a high power semiconductor device due to its superior thermal conductivity, the n-type base region would be used for forming a channel, and a source region is commonly heavily doped for a good contact. Further, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use. *In re Leshin*, 125 USPQ 416.

Regarding claims 14 and 16, Lee et al. further disclose that the low concentration gate region (50) of the second conductivity type (p-type) selectively formed in the upper deposition film (22) has a portion that is in contact with the gate insulation film (60).

Lee et al. in view of Okuno et al. differ from the claimed invention by not showing that the upper deposition film has a thickness within a range of 0.2 μm to 0.7 μm and the low concentration gate region has an impurity concentration higher than $1 \times 10^{15} \text{ cm}^{-3}$ and lower than $5 \times 10^{15} \text{ cm}^{-3}$ (claim 14), and has an impurity concentration of not higher than $2 \times 10^{16} \text{ cm}^{-3}$ (claim 16).

It would have been obvious to one of ordinary skill in the art at the time the invention was made that the silicon carbide semiconductor device disclosed by Lee et al. in view of Okuno et al. may comprise an upper deposition film thickness and a low concentration gate region impurity concentration within the claimed ranges, because the upper deposition film thickness and the low concentration gate region impurity concentration can be controlled to achieve desired silicon carbide semiconductor device

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characteristics to improve performance of the silicon carbide semiconductor device.

Further, the claims are *prima facie* obvious without showing that the claimed ranges of the thickness and impurity concentration achieve unexpected results relative to the prior art range. *In re Woodruff*, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also *In re Huang*, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996) (claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also *In re Boesch*, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and *In re Aller*, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

Response to Arguments

6. Applicants' arguments with respect to claim 13 rejected under 35 USC 102(b) as anticipated by Okuno et al. have been considered but are moot in view of the new ground of rejection.

7. Applicants' arguments filed April 27, 2010 regarding rejection of claim 13 under 35 USC 103 over Lee et al. in view of Okuno et al. have been fully considered but they are not persuasive.

Applicants argue that "Applicants submit those citations in Lee differ from the claimed features as the cited arbitrary portion of 20 between the two p⁺ regions does not correspond to the claimed "high concentration gate region that is adjacent to a non-

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implanted portion that is an exposed part of the upper surface of the lower deposition film" and at the same time correspond to "a low concentration base region formed on a non-implanted region and having a greater width than the non-implanted portion", and that "moreover, the element in Figure 1 of Lee above the portion between the two p^+ regions is **not wider than** that [sic] portion between the two p^+ regions, and thereby clearly a low concentration base region formed on a non-implanted region and having a **greater width** than the non-implanted regions is also neither taught nor suggested by Lee". (1) Merriam-Webster dictionary defines "adjacent" as "not distant" or "nearby", and "portion" as "an often limited part of a whole". Therefore the limitation "the high concentration gate region being adjacent to a non-implanted portion" does not necessarily suggest that "the high concentration gate region" is adjacent to and in contact with the "non-implanted portion", wherein the "non-implanted portion" can be any arbitrarily selected portion of layer 20 between p^+ regions in Lee et al. (2) An arbitrarily selected central portion of layer 20 between p^+ regions in Lee et al. having a smaller width than a width of a low concentration base region (portion of 22 between two p^- regions) is an exposed part of an upper surface of a lower deposition film (20). (3) The low concentration base region (portion of 22 between two p^- regions) is clearly formed on the non-implanted portion, which is an arbitrarily selected central portion of layer 20 between p^+ regions.

Okuno et al. and Lee et al. do not disclose that the non-implanted portion is adjacent to and in contact with the high concentration gate region and another high

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concentration gate region formed in the lower deposition film. An amended claim drawn to this limitation may likely overcome rejection over prior art of record.

Conclusion

8. Applicants' amendment necessitated the new ground of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAY C. KIM whose telephone number is (571) 270-1620. The examiner can normally be reached on 7:30 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. K./

Examiner, Art Unit 2815

May 26, 2010

/Kenneth A Parker/

Supervisory Patent Examiner, Art Unit 2815